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PATENT APPLICATION
ATTORNEY DOCKET NO. LMRX-P032/P1205

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: KIM et al Serial No.: 10/804,430 Filed: March 19, 2004 Title: METHOD FOR THE OPTIMIZATION OF SUBSTRATE ETCHING IN A PLASMA PROCESSING SYSTEM	Group Art Unit: 1765 Examiner: UNASSIGEND Docket: LMRX-P032/P1205 Confirmation No.: 7228 **CERTIFICATE OF MAILING** I hereby certify that this correspondence is being deposited with the US Postal Service as First Class Mail in a postage-paid envelope addressed to the Commissioner for Patents, P.O Box 1450, Alexandria, VA 22313-1450 on March 3, 2005. Signed: /Hanh H. Bui/ Hanh H. Bui

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449 may be material to the patentability of the above-identified patent application. Applicants submit the list of these references in compliance with their duty of disclosure pursuant to 37 CFR §§ 1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is believed to be filed before the mailing date of a first Office Action on the merits. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-2284 (Order No. LMRX-P032).

Respectfully submitted,
By: __/Joseph Nguyen/____
Joseph Nguyen
Reg. No. 37,899

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INFORMATION DISCLOSURE STATEMENT

OTHER DOCUMENTS

Examiner Initials	Cite No.		T
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	2	Hu et al., "Resist Stripping for Multilevel Interconnect Integrating Low-k Dielectric Material", February 2000, AVS First International Conference on Microelectornics and Interfaces	
	3	Chhambra et al., "Interconnect Challenges and Strategic Solutions", February 2, 2002, Future Fab Intl. Volume 12, Issue 17, http://www.future-fab.com/documents.asp?d_ID=912	
	4	Singer, Peter, "Dual-Damascene Challenges Dielectric Etch", August 1999, Semiconductor International, http://www.semipark.co.kr/upload1/Dual-Damascene%20Challenges%20Dielectric%20Etch.pdf	
	5	Schmid et al., "A Novel Oxazole Based Low k Dielectric Addresses Copper Damascene Needs", Semiconductor Fabtech 12th edition, pp. 231-235, http://www.semiconductorfabtech.com/journals/edition.12/fabtech12.pdfs/ft12_pg231.pdf	
	6	Peters, Laura, " Solving the Integration Challenges of Low-k Dielectrics", November 1999, Semiconductor International 22, No. 13, pp. 56-64.	
	7	Lassig et al., "Selective Removal Strategies for Low k Dual Damascene", December 2001, Semiconductor Fabtech Edition 15, pp. 185-190	
	8	Ramalingam et al., "Photoresist Trimming: Etch Solutions to CD Uniformity and Tuning", September 2002, Semiconductor International Volume 20, Issue 5	
	9	Wolf, "Overview of Dual Damascene Cu/Low-k Interconnect", August 2003, International SeMaTech	
	10	Mo Koo, "Design and Process Issues of Junction- and Ferroelectric- Field Effect Transistors in Silicon Carbide", 2003, KTH, Royal Institute of Technology Department of Microelectronics and Information Technology Device Technology Laboratory, ISRN KTH/EKT/FR-2003/1-SE	

Examiner Signature		Date Considered	